CMOS compatible fabrication methods for submicron Josephson junction qubits

A.Potts, G.J.Parker, J.J.Baumberg and P.A.J.de Groot

Abstract: The authors have developed two distinct processes for the fabrication of mesoscopic Josephson junction qubits that are compatible with conventional CMOS processing. These devices, based on superconducting $Al/Al_2O_3/Al$ tunnel junctions, are fabricated by electron beam lithography using single-layer and multi-layer resists. The new single-layer resist process is found to have significant advantages over conventional fabrication methods using suspended tri-layer shadow masks. It is simpler and more accurate to implement, and avoids the significant areas of redundant metallisation that are an unavoidable by-product of the tri-layer shadow mask method.

1 Introduction

The discoveries of algorithms for fast factorisation [1] and database searching [2] have led to increasing interest in the area of quantum computing. Over recent years an ever-increasing number and variety of experimental systems have been proposed and studied [3–6], yet all have so far met with only limited success. This is partly because the predicted hardware requirements, while modest in comparison with existing classical computer architectures, still present daunting experimental challenges. Most notable of these is the realisation that any physical implementation of a quantum computer must balance the requirements for an isolated well defined quantum system, with the need to couple, scale and measure that same system [7]. To build a functional quantum computer, one needs to fabricate a system of many thousands of these quantum bits (qubits) that satisfy five performance criteria outlined by DiVincenzo [7]. This 'checklist' represents the yardstick by which the relative success of all quantum computation systems must be measured.

Of the various experimental systems currently under investigation, one of the most widely studied is nuclear magnetic resonance, or NMR [3, 4]. However, while such systems benefit from low decoherence due to their weak environmental coupling, they do not appear to be readily conducive to large-scale integration. Quantum dots [5] and ion traps [6] on the other hand are currently limited by system nonuniformity and controllability, while most sytems based on semiconductors are also limited by their coherence times. Indeed, it is these competing demands for low decoherence (and system isolation) and measurability (by coupling the system to the environment) that is at the heart of most of the technological difficulties; for while low decoherence is essential if a quantum computer is ever to exhibit the necessary degree of quantum superposition and entanglement, any practical system requires the individual qubits to be coupled together for logic operations, and to the environment for input/ouput operations.

In 1997 Shnirman *et al.* [8] proposed a system of qubits based on mesoscopic Josephson junctions. They argued that, because of their solid state nature, macroscopic phase coherence and similarity to conventional semiconductor devices, quantum circuits based on superconducting devices could potentially combine the scalability and measurability of silicon transistors with the phase coherence and quantum properties of superconductors. Such Josephson junction qubits could be designed around two basic nanostructures: the single electron transistor (SET) and the superconducting quantum interference device (SQUID).

The SET consists of a 'quantum box' sandwiched between two tunnel junctions, the eigenstates being the different charge states of the box. For the system to operate as a (charge-coherent) qubit it must be designed so that only the two lowest charge states are occupied. These states, denoted $|0\rangle$ and $|1\rangle$, are the uncharged state and the lowest charged state, respectively. This is achieved by designing the size of the box so that its capacitance C is so small ($\sim 10^{-15}$ F) that the charging energy $E_c = q^2/C$ becomes comparable with the other energy scales of the system (e.g. the Josephson coupling energy E_J) but is significantly larger than the noise threshold kT. A superposition of the two eigenstates is then achieved by appropriate biasing of the quantum box using an adjacent gate electrode. In a SQUID the tunnel junctions are in parallel and form a superconducting loop. Now it is the magnetic flux through the loop and the associated circulating super-currents that are quantised and form the basis of the eigenstates $|0\rangle$ and $|1\rangle$ in a (phase-coherent) qubit.

In 1999 Nakamura *et al.* [9] demonstrated for the first time a prototype charge-coherent qubit based on a single-Cooper-pair quantum box. While the relatively low Q-factor (~36) meant that this was still a long way from being a practical device, it nevertheless represented a significant leap forward in quantum technology. Subsequently, other workers have demonstrated macroscopic quantum super-

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position in the eigenstates of superconducting rings [10, 11]. However, it is not yet clear how such structures will be affected by quantum decoherence arising from both interactions with the environment and inter-qubit coupling. It is possible that such effects may place an effective limit on the maximum size of such quantum circuits or their operational capabilities. In this case, hybrid architectures, which attempt to harness the relative advantages of both quantum and conventional electronics, may be the way forward. Perhaps more significantly, structures such as these, which would be based on current fabrication technologies, would be cheaper to implement because of reduced development costs.

It is for these reasons that we propose two distinct fabrication schemes for Josephson junction quantum circuits that are not only compatible with current CMOS fabrication processes, but also use such processes. By doing so it is hoped that the two technologies may ultimately be integrated at some point in the future so that the many decades of innovation in silicon microelectronics can be applied directly to the new technologies.

2 Fabrication processes

The design parameters of Josephson tunnel junctions are determined by the requirements imposed on E_J and E_c (both of which must be less than kT_c). This limits the area of the tunnel junctions to less than about $200 \times 200\,nm^2$ and their thicknesses to ~2nm. Using electron beam lithography and other nanofabrication technologies it is, however, possible to fabricate such junctions reliably, thus making Josephson junction qubits a realistic possibility. The most commonly used metals for such junctions are aluminium and niobium because of the purity of their superconducting states and their (relatively) high transition temperatures (T_c = 1.2K and 9.3K, respectively). Of the two, aluminium is the more convenient to use because of its low melting temperature, its insulating native oxide, and its compatibility with silicon CMOS processing.

Mesoscopic $Al/Al_2O_3/Al$ tunnel junctions are usually formed from successive evaporations of Al through a lithographically defined mask with a controlled oxidation step being performed between the two evaporation stages. Because the thickness and quality of the tunnel junction is critical for the performance of the Josephson devices, accurate control of the oxidation step is essential. This oxidation process is further complicated, however, because the required Al_2O_3 thickness is usually much less than the thickness of the native (natural) Al_2O_3 surface layer on Al. Consequently, accurate control of the Al_2O_3 thickness can only be achieved using an in-situ technique [12] where the reactive aluminium from the first evaporation is exposed to O_2 at a fixed concentration and pressure for a given time, and then the second aluminium evaporation is performed without breaking the vacuum in the deposition chamber. However, because only one lithography step can be performed using this technique (at the start of the process), a method must be found by which the second evaporation does not merely replicate the pattern of the first, but adds to it, with a junction being formed where the two metallisations meet.

We have developed two different CMOS-compatible processes to accomplish this. Our first process uses a combination of angled evaporations and a suspended shadow mask similar to methods reported previously by other workers [13, 14]. Fig. 1 shows the schematic arrangement for a shadow mask and how, when used in conjunction with angled evaporations, tunnel junctions can be formed. The fabrication process is based on a tri-layer resist system. We have implemented such a system using 1.1μm of poly(dimethyl-glutarimide) resist (PMGI) on which we have deposited 50–100nm of titanium. The third (top) layer in our trilayer system is 300nm of UVIII resist. This is patterned by direct-write electron beam lithography at 30kV and developed in Shipley MF322 developer for two minutes. The resulting pattern in the UVIII resist is then transferred to the titanium layer by dry etching in SF_6 at 100W for between 150 and 250 seconds. The final step is the isotropic removal of the UVIII resist and the simultaneous undercut of the PMGI by plasma etching in oxygen, to form a free-standing titanium shadow mask approximately 1μm above the substrate surface. Aluminium is then evaporated through this mask at two different angles (usually ±30°) with an intermediate oxidation step performed between these evaporations. The final process step is the removal (or lift-off) of the mask layer using the solvent N-methyl-pyrrolidinone (NMP). An example of a SQUID fabricated using this method is shown in Fig. 2. In this scanning electron micrograph (SEM) the two distinct layers of metallisation are clearly visible, with the lateral offset between the layers being approximately 1μm.

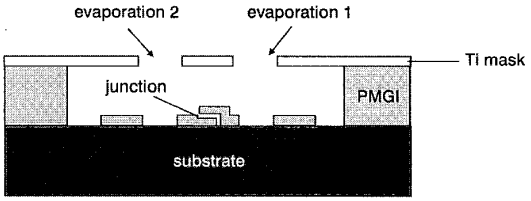

Fig. 1 *Schematic diagram of the cross-section through a shadow evaporation mask showing how by performing two successive evaporations at different angles a junction can be created*

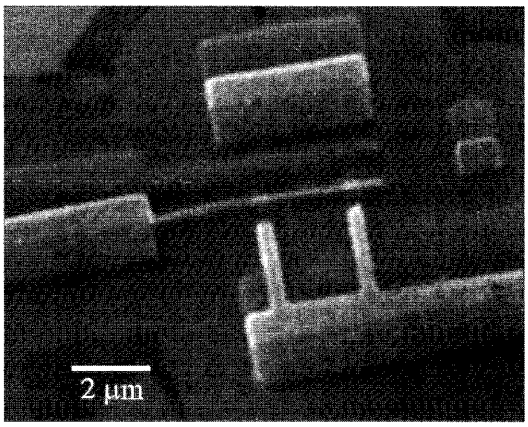

Fig. 2 *SEM image of a SQUID fabricated using the suspended shadow-mask method*
The two evaporations (offset by 1μm) can clearly be seen

The main disadvantages of this fabrication process are the critical limits it places on the accuracy of the PMGI resist thickness and the angles of evaporation. As a result the dimensions of the final structure will depend as much on these parameters as they will on the dimensions of the lithographically defined pattern. In addition, however, the process is also limited by the mechanical and thermal stability of the free-standing titanium shadow mask. This has implications for the future development of quantum circuits where reducing device dimensions and increasing device packing density may require ever thinner shadow masks that are free-standing over ever greater distances.

To overcome these difficulties we have developed a unique process based on a single layer of UVIII resist which, while still using angled evaporations, allows metal to be selectively deposited in different parts of the pattern. By the use of high aspect ratio trenches in the patterned resist layer it is possible to selectively deposit metal in two orthogonal directions. Fig. 3 shows the principle for a basic cross-type structure and an evaporation angle θ. By orienting the wafer such that the angled evaporation is directed parallel to one trench we can ensure that during the first evaporation the metal will reach the bottom of that trench. However, if $\tan(\theta)$ is less than the aspect ratio of the trenches, no metal will reach the bottom of the trench oriented in the perpendicular direction. The result is that a junction can be formed at the centre of the cross by oxidising the surface of the metallic film, and then rotating the wafer by 90° about an axis perpendicular to the plane of the wafer before performing the second evaporation. In this way the position and geometry of the tunnel junction is controlled entirely by the lithographic design and not by the angle of evaporation or the exact thickness of the resist. The process is also no longer limited by the mechanical and thermal stability of the masking layer.

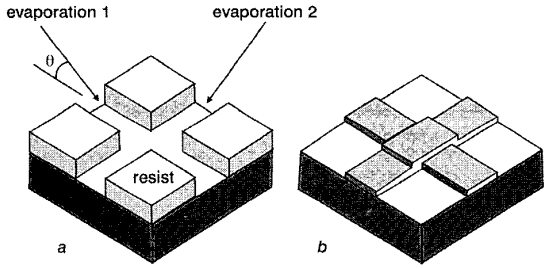

Fig. 3 *Schematic diagram of the single resist layer process*
a Patterned resist on a substrate showing the directions of the two evaporations
b The resulting metal tracks after lift-off

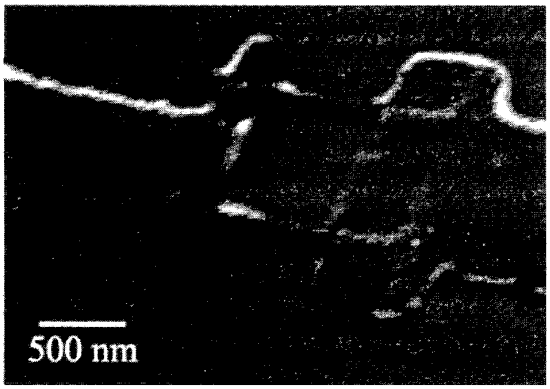

Fig. 4 *SEM image of a SQUID fabricated using the orthogonal evaporation method showing the two distinct levels of metallisation*

Using this technique we have successfully fabricated single electron transistors, charge-coherent qubits and SQUIDs (Fig. 4) for use in quantum circuits. Fig. 5 shows a scanning electron micrograph of a charge-coherent qubit also fabricated using the orthogonal evaporation technique. It is similar in structure to that reported by Nakamura *et al.* [9]. The labels 'JJ' indicate the positions of the Josephson junctions, and at those points the overlap of the two aluminium metallisation layers (as described in Fig. 3) can be clearly observed. It is also noticeable that the final device does not feature the significant areas of redundant metallisation that is a necessary by-product of the shadow-mask method (see Fig. 2).

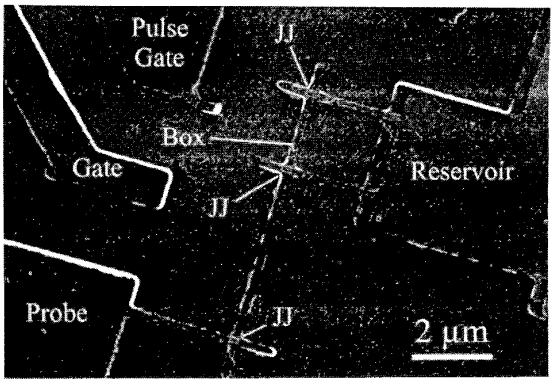

Fig. 5 *SEM image of a charge-coherent qubit fabricated using the orthogonal evaporation method, showing the Josephson junctions (JJ), the gates and the quasi-particle reservoir*

3 Summary

The two distinct fabrication processes described above are each CMOS-compatible. Both use standard resists and thin films, so the resulting quantum devices could in principle be integrated with conventional microelectronic circuits at some point in the future into hybrid devices (if required). We have also shown that the new fabrication process based on orthogonal angled evaporations has significant advantages over existing fabrication methods for nano-scale Josephson junction qubits using shadow evaporation masks. This is partly due to its simplified fabrication scheme, which requires only a single resist/thin film deposition; but a more significant advantage is the greater flexibility of evaporation angle that this method permits. As a result, the orthogonal evaporation method is more tolerant of device processing errors.

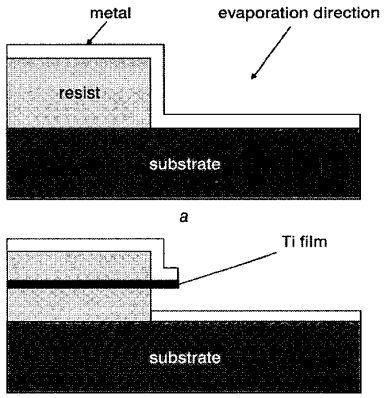

Fig. 6 *Schematic diagram of the resist cross-sections used in the lift-off process*
a Continuous metal layer forms on the resist sidewall, thereby preventing successful lift-off
b Tri-layer system with undercut lower resist layer eliminates this problem

Despite this there are some disadvantages in using this method. For example, it restricts the flexibility of the device designer in deciding how and where the Josephson junctions are positioned, although the shadow mask method is not without drawbacks in this respect either. A more significant disadvantage, however, is the effect the angle of evaporation has on the yield of the final lift-off process (used to strip the UVIII resist and with it the areas of unwanted metallisation). This process is performed by immersing the sample in acetone. As the UVIII resist dissolves, the

unwanted metal will float clear of the device surface. Unfortunately, because of the large angle of evaporation, there will inevitably be areas of contact between the metal at the bottom of the trenches and the metal on top of the resist. This arises from a build-up of evaporated metal on one sidewall of the trench (see Fig. 6*a*) and will prevent satisfactory lift-off being achieved unless corrective action is taken. One solution is to use a bi- or tri-layer resist (similar to the resist layers used for the shadow mask method) with a significant undercut profile (Fig. 6*b*). This will ensure that the metal on the sidewall will be discontinuous and thereby pose no threat to the success of the lift-off process.

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